Abstract of the Disclosure

NON-SYNCHRONOUS HARDWARE EMULATOR

A hardware emulator chip contains an array of cells and a programmable interconnection array. Each cell performs only a single logic function, which is configurable. The chips run asynchronously to one another, and within each chip cells are enabled by a sequential wave signal, which enables successive logical rows of cells. Within the chip, it is possible to connect any arbitrary cell output to any arbitrary cell input. Preferably, a set of off-chip connections is made possible by time-multiplexing the output of each subset to the wave signal. In one embodiment, full interconnection of cells within a chip is provided by providing a time-multiplexed programmable array of interconnect switches, the setting of each switch changing with each successive wave. In a second embodiment, full interconnection of cells within a chip is provided by providing a programmable array of interconnect switches. The hardware emulator described herein may thus be viewed as a hybrid of the FPGA type emulator and the time-multiplexed processor array emulator.